μMaxPak Power Package
by Semiconductor Packaging Solutions

Near Chip-Scale SMD Enabling High Speed & Efficient Power for Wide-Band-Gap Devices, and even Hi-Performance Silicon Devices

μMaxPak Enables

- High Current, Voltage & Speed Power Devices
- Optimum Performance & Efficiency for power GaN & SiC devices, and many Si power devices
- Maximum Power Density & Multiple power devices
- Smart-Power with easy Vertical & Lateral Integration
- Utilizes Commercial DFN/QFN Platforms with both Leadframe & Laminate based molded pkgs

Proprietary μMaxPak Architecture
(U. S. Patent 9,214,416 Issued 12/15/15)

- Leadless(DFN/QFN) & wirebondless SMD packages with exposed power die in leadframe or laminate bottom-side cavity(s), enabling double-side assembly
- Over-molded hi-speed power package with controlled pre-testable performance & parasitics
- Ideal for multiple paralleled power die and/or multiple switches in HB, FB, 3P, PS, PFC & more
- Accommodates Smart-Power with integrated top-side gate-drivers, cascode, isolators & other components/functions.
- Provides lowest R, L & Rjc, and highest power density based on optimum geometric configurations
- Top & bottom die heat transfer to mother-board, and optional top-side heatsinking
- Accommodates small UL pollution 1 spacing for LV, 600V, 1200V & higher products, with proper under-fills, coatings, etc.

μMaxPak Basic Configurations

- Bump & LGA power die with paralleled die/switch & multi-switch, with both lateral & vertical die.
- Common switch configurations are single-switch(SS), Half-bridge(HB), Full-bridge(FB) & Three-phase bridges(3P)
- Smart-Power with Integrated gate-drivers, cascode, isolators & protection circuits are advantageous, and further increase system power density
- **Basic μMaxPak Configurations & Features**

  Standard Type: Power Die Gate & Source Up (Slide 5, 8 & 13)

  Inverted Type: Power Die Gate & Source Down (Slide 6)

  Smart Type: Power Die with integrated supporting functions & components (Slide 13 & 15)

  Thin Type: Inverted with Top & Bottom Heatsinking (Slide 6)

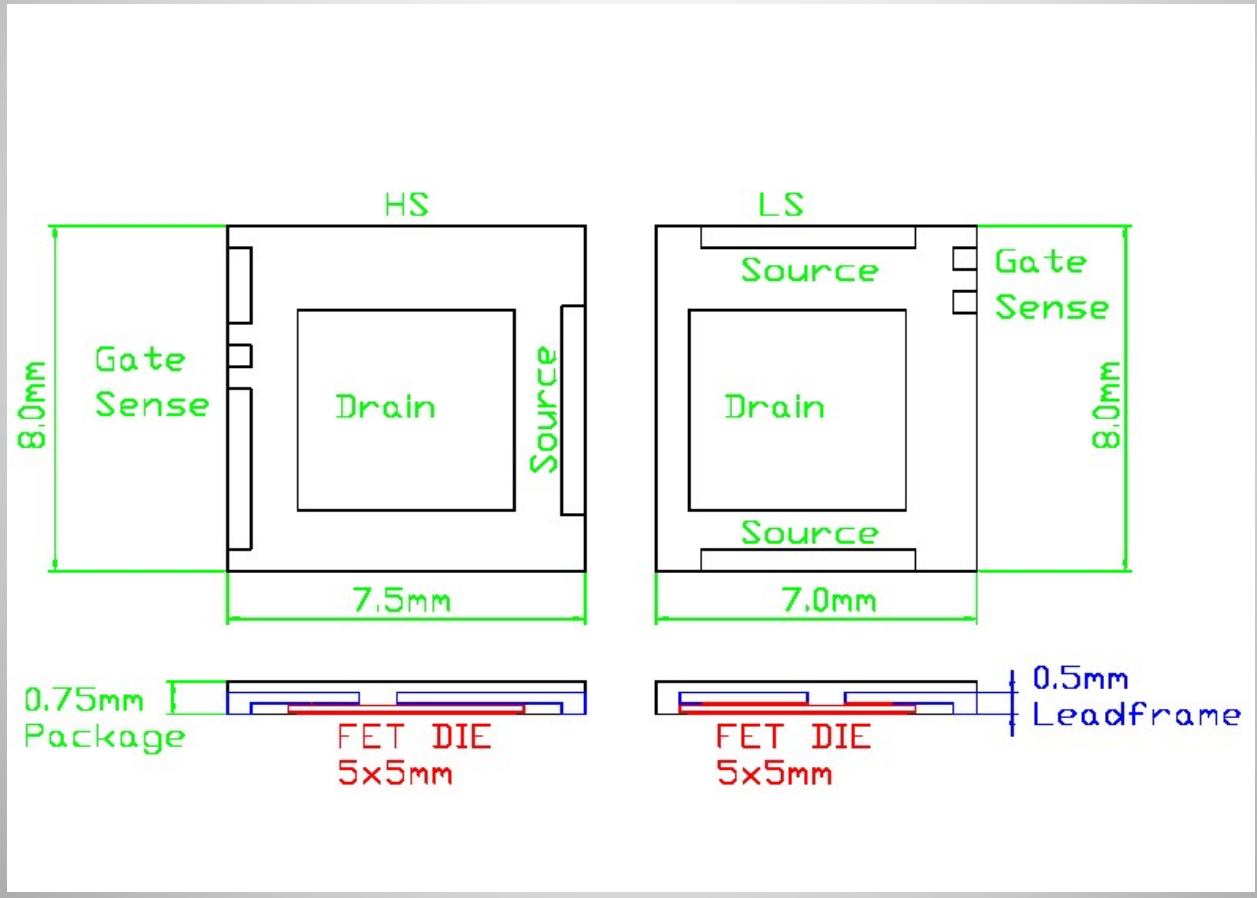
  All Types: Leadless SMD, single/multiple die, wirebondless & leadframe/laminate option

  Combinations: Examples are Standard-Smart Type(Slide 13) & Inverted-Thin Type(Slide 6)

μMaxPak Standard
Hi-Side & Lo-Side Switches
(Complementary μMaxPak Pair for Half-Bridges)

Bottom View

Cross-Section

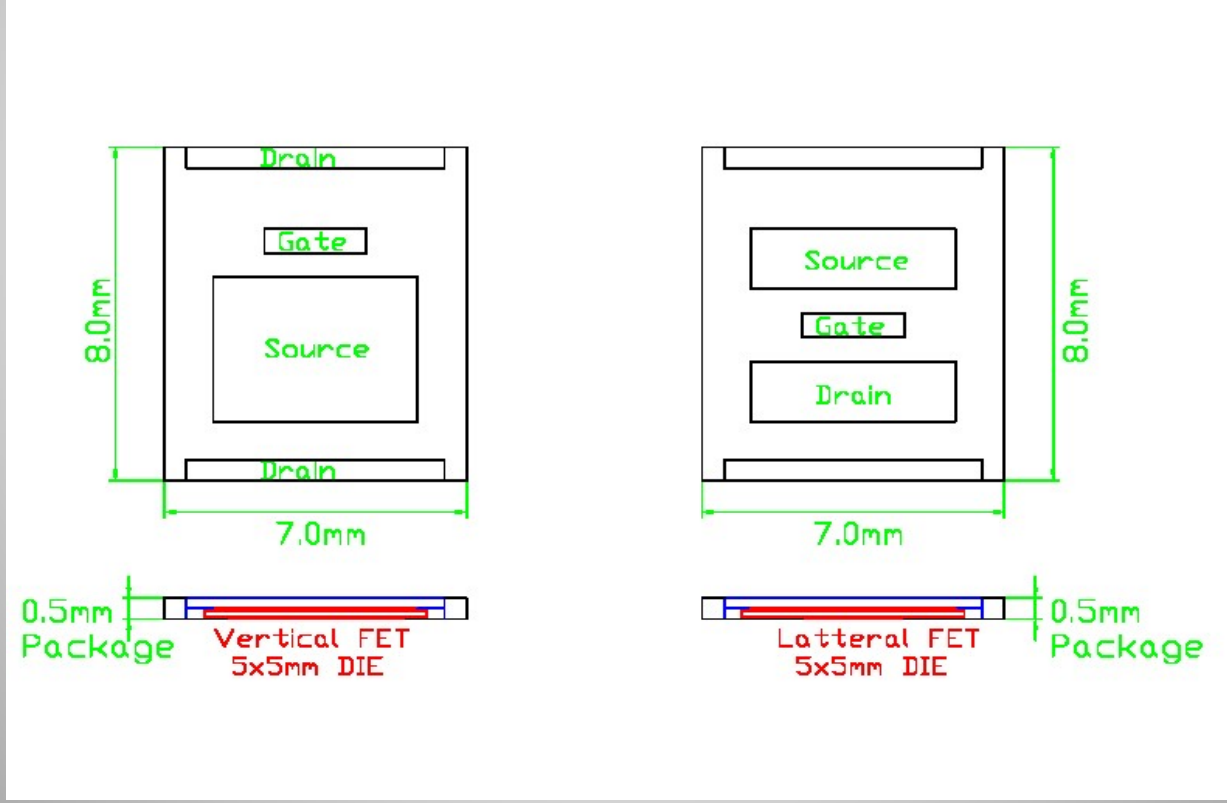


μMaxPak Inverted Thin-Type Single-Switch with Vertical & Lateral Die, Cross-Section & Bottom Pads

1. Enables Top & Bottom Heatsinking/Cold-plate access for Robust EV/HEV
2. The 5x5mm 100A/650V die can be paralleled within μMaxPaks for higher currents

Bottom View

Cross-Section



Symbiotic WBG & μMaxPak Relationship

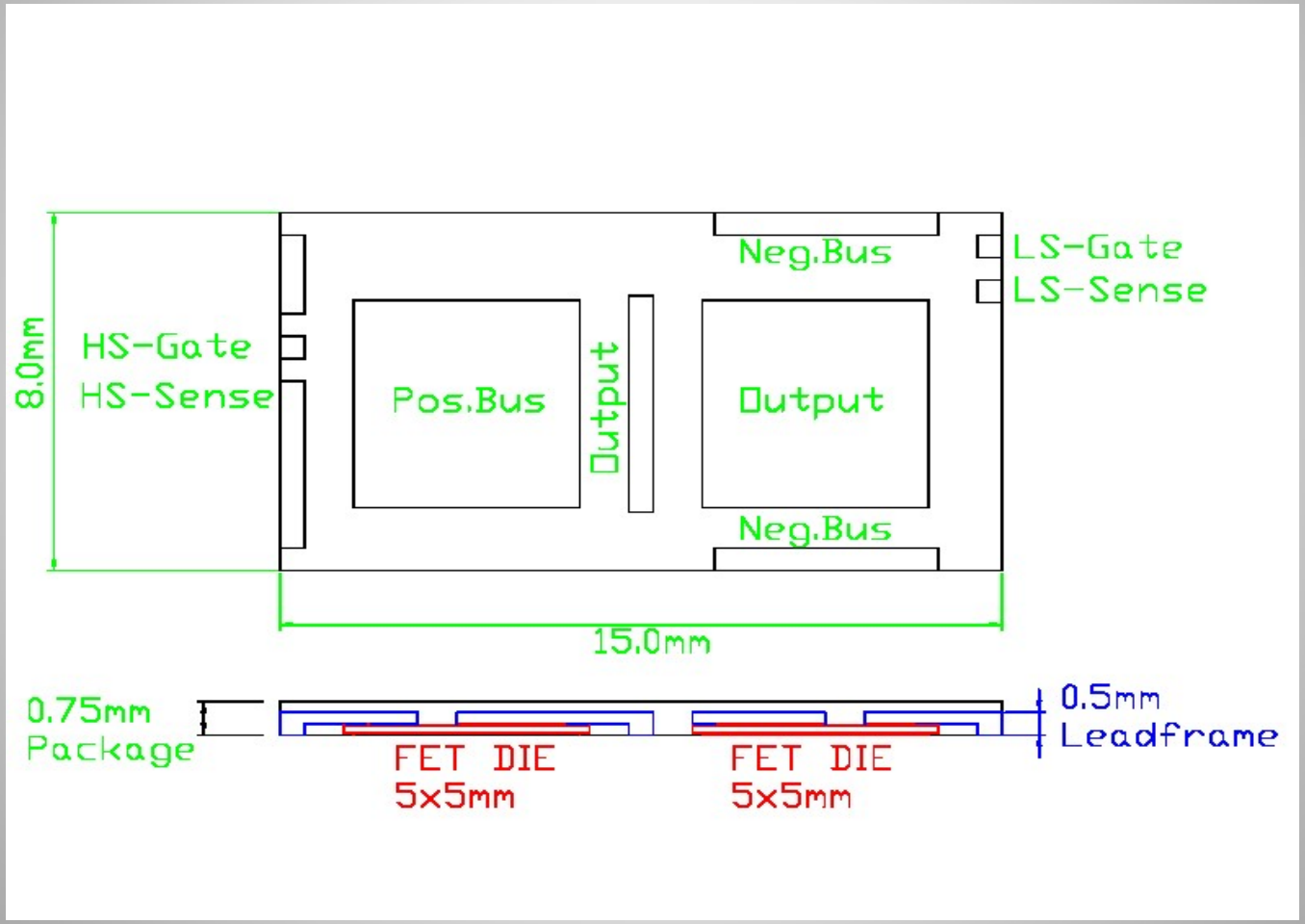
- Power die size on Cu typically limited by CTE mismatch, typically to 6x6mm
- WBG's die power density die can be >x10 Si die, or <1/10th Si die size for a given output power
- Die directly on μMaxPak Cu minimizes R, L & Rjc, reducing conduction losses & junction temperatures
- Low L μMaxPaks enable hi-speed switching & can reduce switching losses & junction temperatures
- μMaxPak increases WBG efficiency, enabling higher power die
- WBG high power density & efficiency are both "needed" & "enable" small μMaxPak architecture

µMaxPak12x8mm HB Layout

(5x5mm Hi-side & Lo-side die can be 600V/100A or 1200V/50A)

Bottom View

Cross-Section



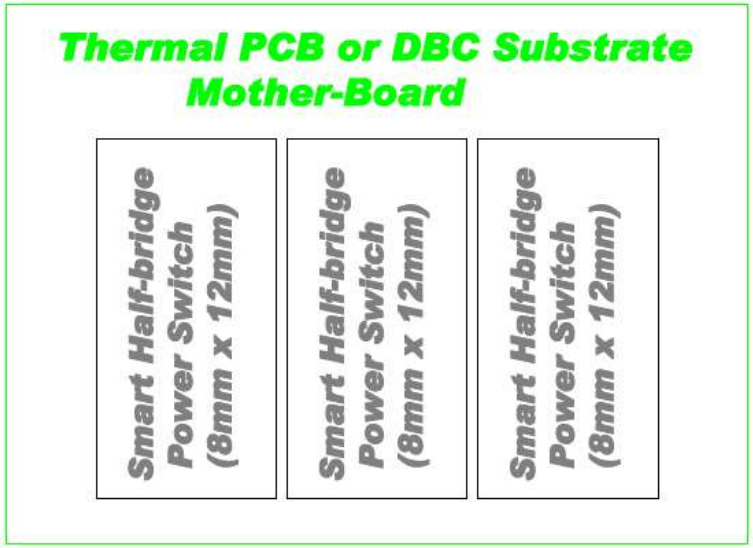
μMaxPak HB,FB & 3P Potential Performance

(600V/100A & 1200V/50AμMaxPak12x8x1mm with 5x5mm GaN die)

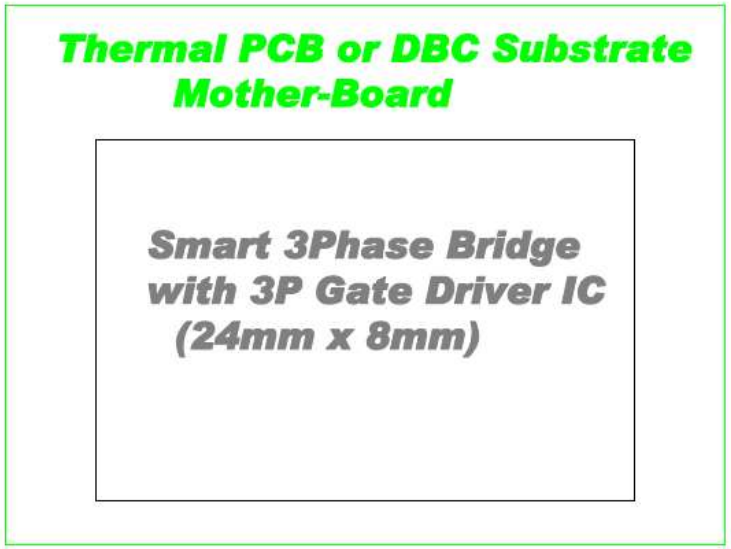
- HB configuration reduces hi-current loop L & R, reduces HV spacing & provides maximum power density
- Inductance: 0.1-0.2nH (HB pkg +/- loop)
- Switch Speed: >100MHz (600V/100A swt)
- Resistance 100-200mohms (HB pkg +/- loop)
- Thermal Resistance: Tjc <0.1C/W (Pkgs w 5x5mm die)
- Maximum Temperature: Tj=185A (higher with hi-temp mat'ls)
- UL Pollution 1 Pad Min. Spacing: Accommodates 230VAC/ 650Vp, 460VAC/1200Vp and higher

3Phase Inverters with three 600V/100A HB μMaxPak, and a Complete 600V/100A 3Phase μMaxPak

(both require Thermal Mother-Board for full performance)



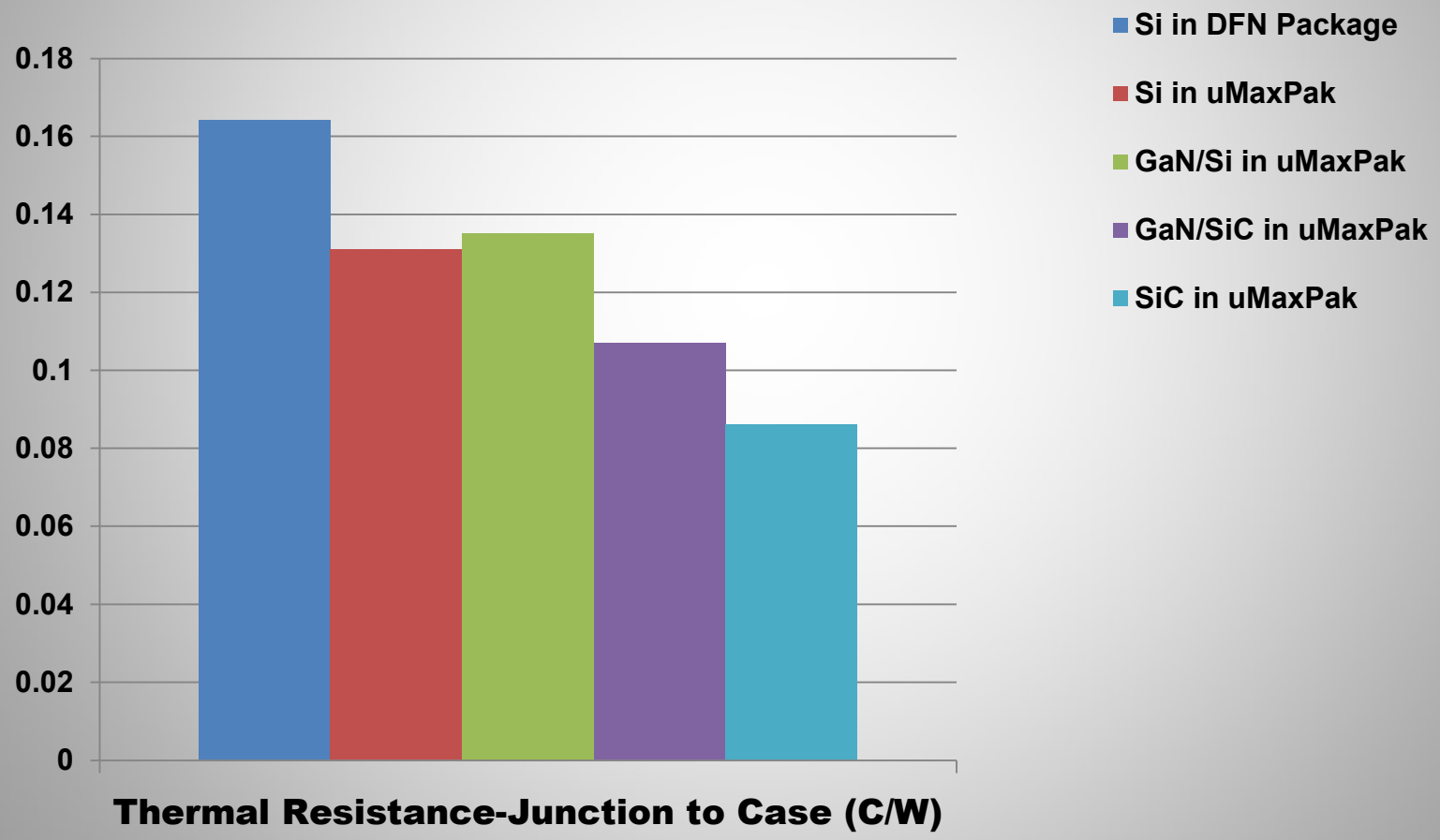
Three μMaxPak HB each with two 5x5mm Power Die(Si-FET, Si-IGBT, GaN & SiC) and a Bump-chip HB Gate-driver



μMaxPak 3Phase Bridge with six 5x5mm Power Die(Si-FET, Si-IGBT, GaN & SiC) and a Bump-chip 3P Gate-driver

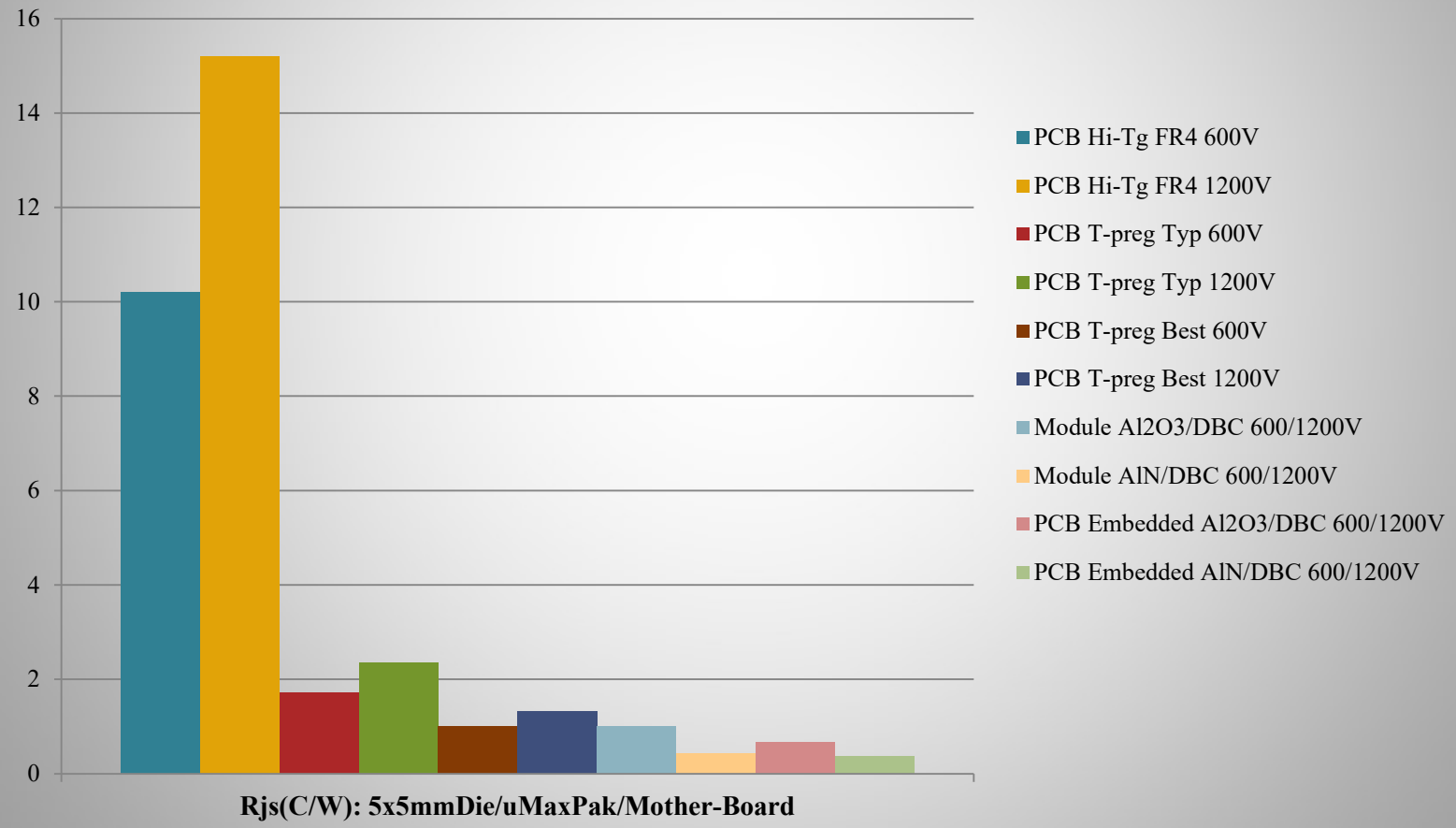
Thermal Resistance(Rjc), Calculated with 5x5mm Die in 8x7mm Leadframe μMaxPak

(The case is the bottom-side μMaxPak solder pads)



Thermal Resistance Rjs (junction-to-sink) for 5x5mm Die in 8x7mm μMaxPak Soldered to Thermal Mother-Board

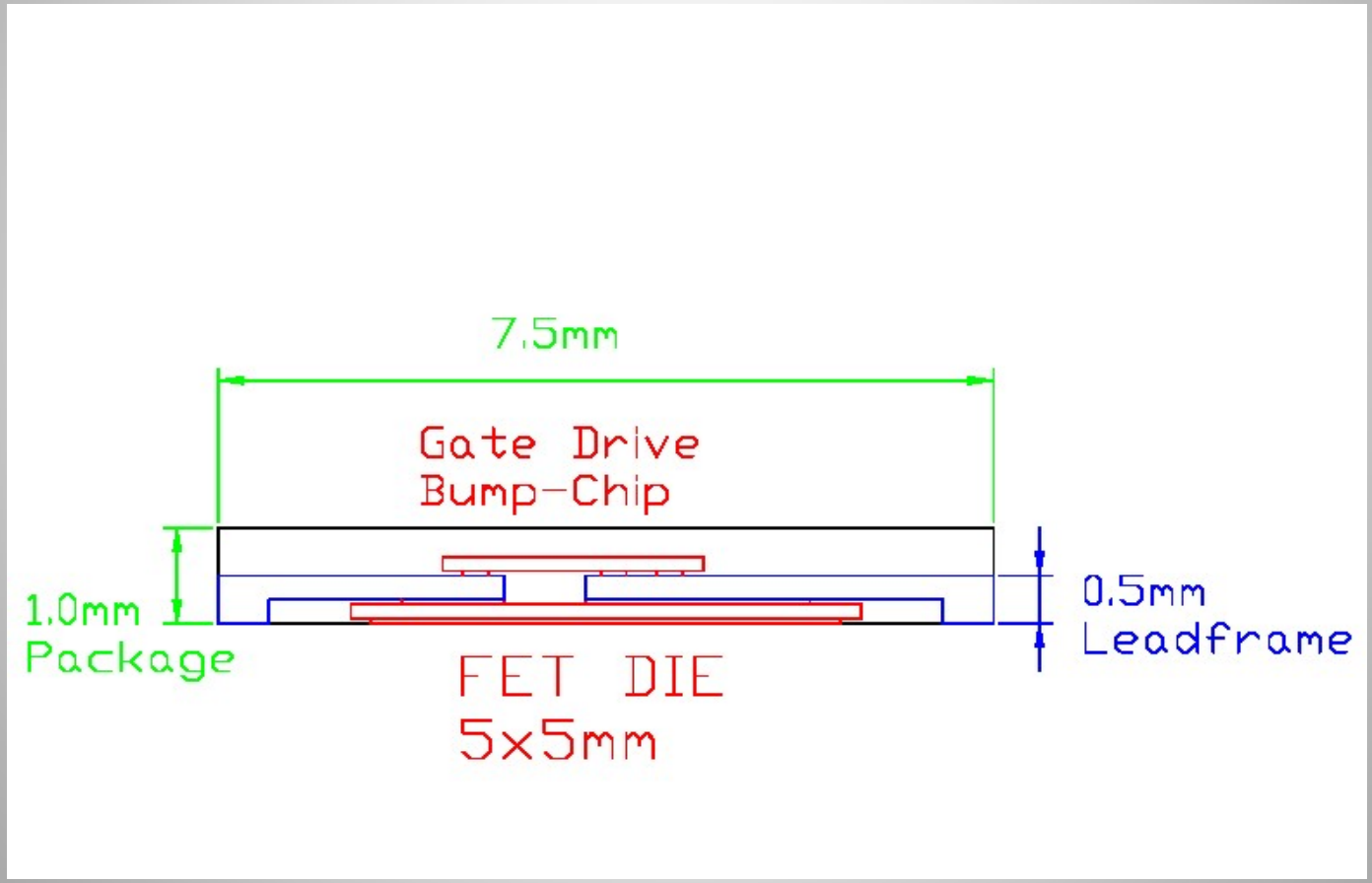
1) Heatsinks(Sinks) are soldered to back of the thermal mother-board
2) Calculations use commercially available thermal pre-pregs(T-preg) & DBC
3) Calculations used isolator thickness rated>3.5/5.0KVAC for 600.1200Vproducts



Rjs(C/W): 5x5mmDie/uMaxPak/Mother-Board

µMaxPak Standard Leadframe Based Smart Switch with Top-Side Gate-Drive IC

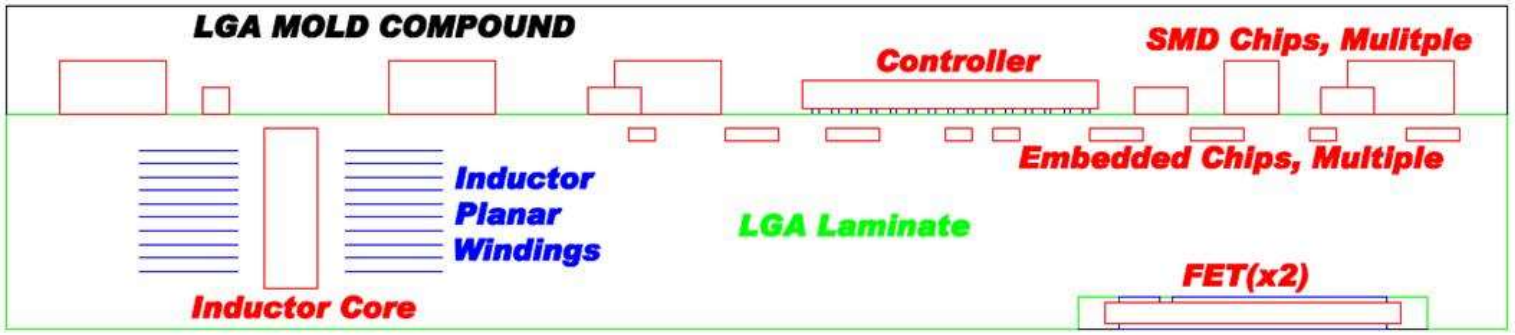
(Gate-driver IC output directly over power FET gate pad)



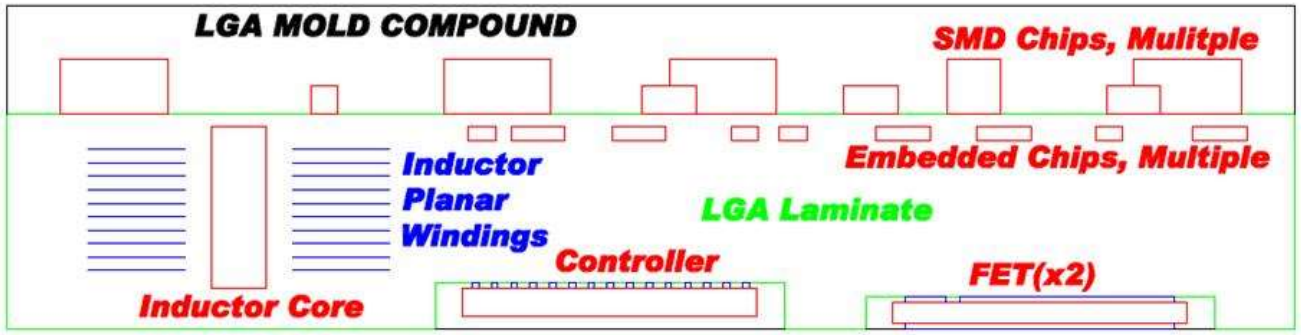
Smart-μMaxPak Integration

- Vertical & Horizontal μMaxPak Integration can provide fully pre-test performance & parasitics. Vertical Integration typically provides best performance
- Integration can increase functions, performance & power density
- Gate-driver outputs directly over gate pads of power die is ideal for hi-speed, lo-noise and paralleled die.
- Increase functionality with cascode, anti-parallel diodes & other switch functions
- Supplementary Horizontal Integration is effective for functions like power supplies, isolators, control and protection. Slide 15 shows examples of DC/DC POD with vertical & horizontal integration in laminate based μMaxPak

µMaxPak Laminate POD Examples
with Vertical & Horizontal Controller integration



µMaxPak POL Concept #1



µMaxPak POL Concept #2

Thin-μMaxPak, Ideal for EV/HEV

- EV/HEV 3P Inverters are generally large, 650Vp and hundreds of amperes output
- Si IGBT & FET usually have power dissipation issues, and associate thermal & reliability issues
- Power GaN & SiC Inverters offer higher efficiency with reduced power dissipation and μMaxPak offer lower Rjc (WBG do have other limitations to be resolved for EV/HEV)
- Thin-μMaxPaks are mechanically & electrically robust, and accommodate top & bottom heatsinks(or cold-plates)
- Top isolation layer can be in μMaxPak or external

μMaxPak as Module Building Blocks

- Very high power switches can exceed P.D. of most thermal PCBs. Thinner embedded DBC can create PCBs with lower Rjc than conventional DBC modules
- μMaxPak can be pre-tested building blocks, which minimize multiple die yield losses. Especially important for evolving GaN & SiC devices
- Pre-tested building blocks can include multiple power die, gate-drivers & other critical functions/components
- μMaxPak module building blocks enable more complete bridges & supporting system functions.
- Module Integration improves performance, parasitics, reliability, external lead isolation, power density, ease-of-use and value-added

μMaxPak vs Existing WBG Packages

- SMD μMaxPak can extend GaN & SiC into ranges which were exclusively module domain, reducing costs & size.
- Todays power WBG devices are primarily packaged in TO220/TO247 with some PQFN. All limit full WBG performance
- Early leadless SMD DFN & LGA packages are being introduced, but sales & performance is limited, and will be insufficient at higher WBG speeds & currents
- Industrial DBC modules are complex, large and expensive(unit, tooling & equipment)

µMaxPak Advantages Over Existing & Emerging WBG Power Packages

(µMaxPak advantages become requirements as current & speed increase towards WBG potential)

WBG Package Type Package Architecture	D^2Pak&TO220-247 Custom Multi-Chip	LGA QFN Lamiante-Based	Power PQFN LF w Solder Clip	µMaxPak Laminate-Base	µMaxPak Leadframe-Base
Parasitcs(L)	High	Moderate	Low	Very Low	Near-Zero
Package Losses(R)	High	Moderate	Low	Low	Lowest
Thermals(Rjc)	Low	Moderate	Low	Low	Lowest
Power Density	Low	Moderate	High	High	Highest
SMD	D2Pak only	YES	YES	YES	YES
Leadless	NO	YES	YES	YES	YES
Wire Bondless	NO	YES & NO	YES	YES	YES
Max BV	600/1200(TO247)	600/1200	600/1200	600/1200	600/1200
Max.Current, 600V(2)	<50A(D2Pak/TO220)	<50A	50A	150A	200A
Max.Current, 1200V(1)	50A(TO247)	<50A	<50A	75A	100A
Switches, Potential	SS	SS/HB/FB/3P	SS/HB	SS/HB/FB/3P	SS/HB/FB/3P
Integration, Potential	Cascode	Cascode/GD/isol/etc	Cascode	Cascode/GD/isol/etc	Cascode/GD/isol/etc
Complexity	High	Moderate	Moderate	Low	Lowest
Manufacturability	Fair	Good	Poor	Good	Good
Value	Poor	Fair	Poor	Good	Best
Cost	Marginal	Low	High	Low	Low

NOTES:

1. µMaxPak is a proprietary DFN/QFN architecture offered with package constraints shown.
2. Typical maximum continuous GaN & SiC currents of available HV SiC & GaN products.
3. µMaxPak highlighted parameters are as good as or better than the best competing packages.
4. To Accommodate GaN and SiC, the TO-220, D2Pak, TO0247, and PQFN assemblies are non-std & complex with multi-components, isolators, etc.

μMaxPak Edge Summary

- Power multichip SMDs are simple, Lo-L, Lo-R, Lo-Rjc, Hi-density and Lo-Cost commercially manufacturable
- Enables optimum hi-speed performance and efficiency for power WBG devices, like GaN & SiC
- Enables multi-chip switches & smart integration with simple construction & proven technology
- User friendly low-cost SMDs on Power PCBs can replace many power modules, and can be building blocks for very high power modules
- Improvements are advantageous for WBG power today, but are essential as WBG devices evolve towards full potential